

paragraphs contain a summary of the substance of those interviews. At the conclusion of the interviews, the Examiner agreed to reconsider the present rejections.

In the Office Action of May 14, 2003, each of the independent claims (Claims 114, 117, and 120) was rejected under 35 U.S.C. § 103(a) as being unpatentable in view of the proposed combination of U.S. Patent No. 6,208,545 to Leedy and European Patent Application No. EP1017100 to Shimoda et al. Applicants respectfully request reconsideration and withdrawal of these rejections because, even if Leedy and Shimoda et al. are combined, the proposed combination does not teach a plurality of layers of memory cells stacked vertically above one another in a single chip, as recited in the claims.¹

As admitted in the Office Action, Leedy fails to disclose a plurality of layers of memory cells stacked vertically above one another in a single chip, and Shimoda et al. was relied upon in an attempt to cure this deficiency. However, Shimoda et al. suffers from the same deficiency as Leedy. Namely, like Leedy, Shimoda et al. teaches a device in which layers of memory cells are bonded together after manufacturing — not stacked vertically above one another in a single chip, as recited in the claims. For example, col. 31, lines 21-24 states that “the substrate 21 and the memory cell array 71, the memory cell array 71 and the memory cell array 72, and the memory cell array 72 and the memory cell array 73 may be *bonded (joined)*” (emphasis added). The following are additional passages that teach that the disclosed memory cell layers in Shimoda et al. are not stacked vertically above one another in a single chip.


¹ In the prior Response, Applicants argued that there was no suggestion to combine Leedy and Shimoda. To the extent that Applicants implied that Shimoda et al. teaches a three-dimensional single chip/monolithic integrated circuit, that implication is hereby expressly withdrawn.

- A. Front page abstract: "... a method for transferring a thin film ... irradiating the separable layer ... so that the thin film device layer on the support substrate is transferred to the substrate 21."
- B. Col 1, lines 51-56: "A three-dimensional device ... in which at least one of the thin film device layers is deposited by a transfer method."
- C. Col 2, lines 4-5: "... in which at least one of the thin film device layers is deposited by a transfer method."
- D. Col 2, lines 6-14: "A three-dimensional device ... in which the transfer method includes ... a thin film device layer on a support substrate ... so that the thin film device layer ... is transferred to a substrate of the three-dimensional device."
- E. Col 6, "Best mode" text describes, once again, the transfer method. Lines 40-46 describe the necessity for transparency to light, as the best mode employs (laser) light to effect the separation of the thin films from the separate transfer source substrates. Once so liberated, the thin films are assembled atop the main recipient substrate to form the 3D device.
- F. Col. 22, lines 26-30: "the transfer source layer 42 formed on the substrate 1 and the transfer source layer 41 transferred to the substrate 21 are bonded (joined) to each other with a conductive adhesive layer 22 therebetween."
- G. Col. 23, lines 1-4: "The substrate 1 is then separated from the substrate 21. Thus, as shown in Fig. 15, the transfer source layer 42 is detached from the substrate 1 and is transferred to the transfer source layer 41."
- H. Col. 23, lines 36-37: "each of the thin film device layers can be fabricated individually"

In summary, because the memory cell layers in Shimoda et al. are not stacked vertically above one another in a single chip, Shimoda et al. does not cure the admitted deficiency in Leedy. Accordingly, Applicants respectfully request reconsideration and withdrawal of the present rejections of the claims. If the Examiner has any questions concerning this Response, he is asked to phone the undersigned attorney at (312) 321-4719.

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Respectfully submitted,



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